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(54) Packaged semiconductor device suitable to be mounted and connected to microstrip line structure board.

(57) A packaged semiconductor device comprises an insulating substrate (2) having an upper surface formed with a plurality of connection pads (6) and an under surface formed with a plurality of external connection members (7) each of which is electrically connected to a corresponding one of the connection pads (4) through a via hole (2A) formed through the insulating substrate (2). An integrated circuit chip (1) is bonded facedown on the upper surface of the insulating substrate (2) so that the integrated circuit chip (1) is electrically connected to the connection pads (6) through solder bumps (9). An electrically conductive cap (3, 41, 42) is covered on the first surface of the insulating substrate (2) so that the integrated circuit chip (1) is encapsulated in a space defined by the insulating substrate and the conductive cap. A back electrode of the integrated circuit chip (1) is electrically connected to the conductive cap.through an electrically conducting element (50A).

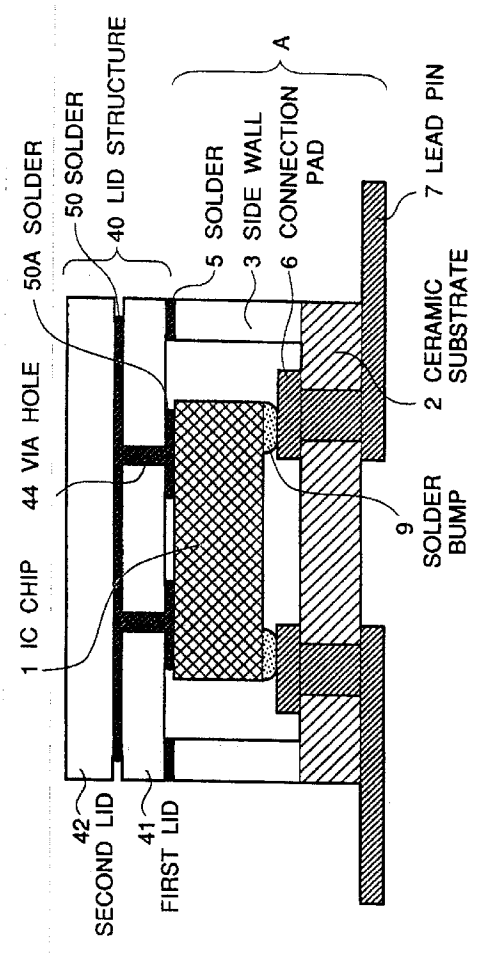


FIGURE 2

EP 0 615 289 A2

Background of the Invention

Field of the invention

The present invention relates to a semiconductor device, and more specifically to a semiconductor device containing an integrated circuit chip packaged in a flip-chip bonding and having a novel structure suitable to be mounted and connected to a microstrip line structure.

Description of related art

At present, high-speed information network systems and satellite communication systems are being rapidly developed, and therefore, a demand for a semiconductor device operating in a high frequency band such as UHF (ultrahigh frequency), SHF(super-high frequency) and EHF (extremely high frequency) is now increasing. On the other hand, FET (field effect transistor), in particular, MESFET (metal semiconductor FET) and HEMT (high electron mobility transistor) formed of a compound semiconductor typified by GaAs, are expected as a device capable of breaking down a limitation in characteristics of silicon bipolar transistors conventionally used in the high frequency band, and practical use of these elements is being promoted.

It has been confirmed that high frequency IC (integrated circuit) chips including GaAsFETs have an extremely high performance. However, packaged or encapsulated high frequency integrated circuit chips cannot, in many cases, exert the excellent performance of the IC chips themselves.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a packaged semiconductor device which has overcome the above mentioned defect of the conventional one.

Another object of the present invention is to provide a packaged semiconductor device capable of exerting an excellent performance of the integrated circuit chips themselves without being impaired.

The above and other objects of the present invention are achieved in accordance with the present invention by a package semiconductor device comprising:

an insulating substrate having a first surface formed with a plurality of connection pads and a second surface formed with a plurality of external connection members each of which is electrically connected to a corresponding one of the connection pads through a via hole formed through the insulating substrate;

an integrated circuit chip bonded facedown on the first surface of the insulating substrate so that the integrated circuit chip is electrically connected to the connection pads through solder bumps, the integrated circuit chip having a back electrode formed on a back surface thereof; and

an electrically conductive cap covered on the first surface of the insulating substrate so that the integrated circuit chip is encapsulated in a space defined by the insulating substrate and the conductive cap,

the back electrode of the integrated circuit chip being electrically connected to the conductive cap.

Specifically, the back electrode of the integrated circuit chip is electrically connected through an electrically conducting element to the conductive cap.

In one embodiment of the package semiconductor device, the conductive cap is composed of a side wall bonded at its lower end to the insulating substrate so as to surround the integrated circuit chip and a lid plate bonded to an upper end of the side wall, and wherein the electrically conducting element is formed of a contact plate having a central region mechanically contacted and electrically connected to the back electrode of the integrated circuit chip, the contact plate also including a peripheral portion sandwiched and electrically connected between the lid plate and the upper end of the side wall.

Preferably, the contact plate is in the form of a lead frame having a plurality of legs radially outwardly extending from the central region, a tip end of each of the plurality of legs being sandwiched and electrically connected between the lid plate and the upper end of the side wall.

In another embodiment of the package semiconductor device, the conductive cap is composed of a side wall bonded at its lower end to the insulating substrate so as to surround the integrated circuit chip and a lid structure bonded to an upper end of the side wall, the lid structure being bonded and electrically connected to the back electrode of the integrated circuit chip through a solder.

More specifically, the lid structure includes a first lid member bonded to the upper end of the side wall, the first lid member having a plurality of via holes formed through the first lid member, and a second lid member bonded to the first lid member through a solder, the solder filling the via holes and extending to a lower surface of the first lid member so as to mutually bond the the first lid member and the back electrode of the integrated circuit chip.

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a diagrammatic sectional view of one

typical conventional packaged semiconductor device;

Figure 2 is a diagrammatic sectional view of a first embodiment of the packaged semiconductor device in accordance with the present invention;

Figures 3A to 3C are diagrammatic sectional views illustrating a process for manufacturing the packaged semiconductor device shown in Figure 2;

Figures 4A to 4D illustrate various via hole patterns formed in the lid member provided in the packaged semiconductor device shown in Figure 2;

Figure 5A illustrates the lid member having the via holes surrounded by the solder spreading limiting area;

Figure 5B illustrates the lid member having the via holes surrounded by the solder spreading limiting dam structure;

Figure 5C illustrates a metallized area formed as the back electrode on the back surface of the IC chip;

Figure 6 is a diagrammatic sectional view of the packaged semiconductor device assembled into an assemble circuit board of the microstrip line structure;

Figure 7 is a diagrammatic sectional view of a modification of the packaged semiconductor device shown in Figure 2;

Figure 8A is a diagrammatic sectional view of a second embodiment of the packaged semiconductor device in accordance with the present invention;

Figure 8B illustrates a pattern of one example of the contact plate provided in the packaged semiconductor device shown in Figure 8A; and

Figure 8C is an exploded sectional view of the packaged semiconductor device shown in Figure 8A.

Description of the Preferred embodiments

Referring to Figure 1, there is shown a diagrammatic sectional view of one typical conventional packaged semiconductor device.

The shown semiconductor device includes a microwave IC (integrated circuit) chip 1 die-bonded on an upper surface of a substrate 2 formed of for example a ceramics. The upper surface of a substrate 2 is covered with a metal cap, which is formed of a side wall 3 air-tightly bonded to a periphery of the upper surface of the substrate 2 so as to surround the IC chip 1 remotely from the IC chip 1, and a lid 4 air-tightly bonded to an upper end of the side wall 3 by means of a solder 5. A plurality of contact pads 6 are formed on the upper surface of the substrate 2 to be located between an IC chip die bonding area and the side wall 3, and a plurality of lead pins 7 are fixed to an under surface of the substrate 2 so as to outwardly extend beyond the substrate. Each of the connection pads 6 is electrically connected to a corresponding one of the lead pins 7 through a via-hole 2A formed through the substrate 2 and filled with an electrically conducting material. Each of contact pads (not shown) formed on an upper surface of the IC chip 1 is connected to a corresponding one of the connection pads 6 through a bonding wire 8.

Examining the above mentioned packaged microwave IC chip, since the bonding wires 8 are formed of a thin metal wire, the bonding wires 8 have a substantial parasitic inductance. The applicant considers that this parasitic inductance inevitably deteriorates the characteristics of the device, particularly in a high frequency. Namely, This is one of major causes preventing exertion of the excellent performance of the high frequency IC chips.

In order to avoid use of the bonding wires, it may be considered to use a so called flip-chip bonding, in which the IC chip is connected through bumps formed of for example gold or solder. In this flip-chip bonding, the IC chip is bonded on a substrate in such a manner that a pad-formed surface of the IC chip is faced down to an upper surface of the substrate. Therefore, no attention is paid to an electrical connection to a back electrode formed on the back surface of the IC chip. Accordingly, this type of package cannot be used for mounting a microwave IC on a circuit board of the microstrip line type having a ground plane which is formed on the under surface of the circuit board and which needs to be connected to the back electrode of the IC. Namely, the flip-chip bonding is not compatible to the microstrip line structure.

In this connection, it may be also considered to make the IC chip into a uniplanar structure requiring no ground plane formed on the back surface of the IC chip. In this uniplanar structure, since all circuit elements including the ground lines are located at the upper surface of the IC chip, even if the IC chip is packaged in the flip-chip bonding, there occurs no problem for connecting to the ground plane formed of the back electrode of the IC chip. However, a transmission line formed in the uniplanar structure inevitably has a loss substantially larger than a microstrip line. Accordingly, this uniplanar structure cannot be applied to a low-noise amplifier IC

Under the above mentioned circumstance, the applicant has succeeded in provide a packaged semiconductor device capable of exerting an excellent performance of the IC chips themselves without being impaired, by the applicant's unique conception which makes it possible to electrically connect the ground plane formed of the back electrode of the IC chip to the ground plane of the microstrip line type board, with using no bonding wire inevitably having a substantial parasitic inductance.

Referring to Figure 2, there is shown a diagram-

matic sectional view of a first embodiment of the packaged semiconductor device in accordance with the present invention. In Figure 2, elements similar or corresponding to those shown in Figure 1 are given the same Reference Numerals, and explanation thereof will be omitted.

As would be seen from comparison between Figures 1 and 2, the IC chip 1 is mounted on the upper surface of the substrate 2 in a flip-chip bonding manner. Namely, the IC chip 1 is flipped, in comparison with the conventional example shown in Figure 1, so that each of the contact pads formed on the faced-down upper surface of the IC chip 1 is electrically connected and mechanically fixed through a bump 9 to a corresponding connection pad 6 formed at the upper surface of the substrate, by using no bonding wire. Accordingly, the structure of a portion "A" under the level of an upper end of the side wall 3 is substantially similar to a corresponding portion of the conventional example shown in Figure 1, except that the IC chip 1 is mounted in a flip-chip bonding manner.

On the other hand, a lid structure 40 of this embodiment has a unique structure substantially different from the conventional example shown in Figure 1. The lid structure 40, air-tightly bonded, namely, sealed to the upper end of the side wall 3 by means of a solder 5, includes a first lid member 41 and a second lid member 42 stacked on the first member 41. The side wall 3 and the first and second lid members 41 and 42 are formed of a metal material, for example, gold-plated Kovar.

A periphery of an under surface of the first lid member 41 is air-tightly bonded to the upper end of the side wall 3 by means of the solder 5, which is formed of for example a gold-tin alloy, and the second lid member 41 is bonded to a substantial whole of an upper surface of the first lid member 41 through a solder 50, which is also formed of for example a gold-tin alloy. In addition, the first lid member 41 has a plurality of via holes 44 penetrating through the first lid member 41, and the solder 50 fills the via holes 44, and furthermore, reaches and bonds to the faced-up back surface of the IC chip 1. Solders 50A flowed over through the via holes 44 bonds between the faced-up back surface of the IC chip 1 and the under surface of the first lid member 41.

With the above mentioned arrangement, the faced-up back electrode of the IC chip 1 is electrically connected through the solder 50 to the lid structure 40, and hence to the metallic cap composed of the lid structure 40 and the side wall 3. Accordingly, if the cap composed of the lid structure 40 and the side wall 3 is used as the ground plane of a microstrip line structure, the shown packaged semiconductor device can constitute a transmission line of the microstrip line structure in which the cap composed of the lid structure 40 and the side wall 3 forms the ground plane and the lead pins 7 form individual signal conductors. Furthermore, since the IC chip 1 is completely hermetically encapsulated by the substrate 2 and the lid structure 40, the finished packaged semiconductor device can be handled similarly to conventional packaged semiconductor devices.

Now, a process for manufacturing the above mentioned packaged semiconductor device will be explained with reference to Figures 3A to 3C.

As shown in Figure 3A, pre-formed solder bumps 9, which are formed of for example Pb·Sn solder or gold, are located on contact pads 9A formed on an upper surface 1A of the IC chip 1. A back electrode (ground electrode) is formed to cover an under surface 1B of the IC chip 1.

Then, the IC chip I having the solder bumps 9 is bonded facedown on the substrate 2 which has been assembled with the side wall 3 and the lead pins 7 as shown in Figure 3B, so that the bumps 9 are directly above corresponding connection pads 6 formed on the substrate 1. All the contact pads formed on an upper surface of the IC chip 1 are simultaneously bonded to the corresponding connection pads 6 formed on the substrate 1 by melting the pre-formed solder bumps 9. Thus, as shown in Figure 3B, the IC chip 1 is bonded to the substrate 2 in the flip-chip bonding.

Thereafter, as shown in Figure 3C, pre-formed solder bumps 5 are put on an upper end surface of the side wall 3, and then, the first lid member 41 is located on the pre-formed solder bumps 5, and further, pre-formed solders 50 are put on the via holes 44 of the first lid member 41, and finally, the second lid member 42 is located on the first lid member 41. The solders 50 are preferred to be formed of gold-tin eutectic crystal.

Suitable heat and pressure are applied onto the stacked first and second lid members 41 and 42 so as to force the first and second lid members 41 and 42 to the side wall 3, so that the first lid member 41 is bonded to the upper end of the side wall 3 by the solder 5, and simultaneously, the second lid member 42 is bonded to the first lid member 41 by the solder 50. Furthermore, the molten solder 50 flows through the via holes 44 onto the faced-up back surface of the IC chip 1, so that the via holes 44 are filled with the solder 50 and the faced-up back surface of the IC chip 1 is bonded to the stacked and bonded first and second lid members 41 and 42 through the solder 50A, as shown in Figure 2.

Here, the amount of the pre-formed solders 50 to be sandwiched between the first and second lid members 41 and 42 before the bonding, is a very significant control parameter. The pre-formed solders 50 have not only a function of filling up the via holes 44 of the first lid member 41 and of air-tightly and integrally forming the package, but also another function of simultaneously electrically connecting the back electrode of the IC chip 1 to the package. Accordingly, the amount of the pre-formed solders 50 must be suf-

ficient to achieve both of the above mentioned functions, but if the amount of the pre-formed solders 50 is too large, the solder flows into a portion of an internal space of the package to which the solder is not to be flowed, and causes a short-circuit within the package.

For realizing a good controllability of spreading of the solder so as to uniformly spread the solder over only a necessary area, the following method is proposed.

First, as shown in Figures 4A to 4D, it is preferred to form a balanced shape and arrangement of via holes 44 so as to ensure that when the first and second lid members 41 and 42 are bonded, the solders 50 are uniformly and smoothly spread and supplied to the under surface of the first lid member 41.

For example, as shown in Figure 4A, a plurality of via holes 44A having the same shape, for example, a circles having the same diameter, can be formed in the first lid member 41 at equal intervals both in a vertical direction and in a horizontal direction. Alternatively, a plurality of linear elongated via holes 44B having the same width and the same length (in a horizontal direction) can be formed in the first lid member 41 at equal intervals in a vertical direction.

Furthermore, a plurality of via holes having different shapes can be formed in the first lid member 41 as shown in Figure 4C. In the example shown in Figure 4C, four L-shaped via holes 44C having the same width are formed to define four corners of an imaginary square, and a square via hole 44D is formed at a center of the imaginary square. In addition, as shown in Figure 4D, a plurality of linear elongated via holes 44F having the same width and the same length can be formed in the first lid member 41 at equal angular intervals to outwardly radially extend from a center region of the first lid member 41.

However, the shape and the location of the via holes 44 are not limited to the shown example, and can be freely determined in the extent capable of uniformly and smoothly spreading and supplying the solders 50 to the under surface of the first lid member 41.

Furthermore, it is preferred to form a construction for restricting the spreading of the solders 50, on the upper surface of the first lid member 41, the under surface of the first lid member 41 and/or the faced-up back surface of the IC chip 1 (on which the back electrode is formed).

For example, as shown in Figure 5A, all the via holes 44A formed as shown in Figure 4A are substantially surrounded by a solder spreading limiting area 46, which is formed of a material having a small or less wetting property to the material of the solder 50. Alternatively, to physically damming up the spreading of the solder 50, the solder spreading limiting area 46 having the small wetting property can be replaced with a dam structure 48 formed on the first lid member 41 so as to completely surround all the via holes 44A, as shown in Figure 5B

Furthermore, a similar effect can be obtained if a metallized area 1C formed as the back electrode on the faced-up back surface of the IC chip 1 is confined so that a non-metallized area is left at a periphery of the back surface of the IC chip 1, as shown in Figure 5C. Since a non-metallized surface of the IC chip 1 has a remarkably low wetting property to the solder material, the solder will effectively spread over only the metallized area.

With the above mentioned various arrangements, it is possible to prevent an extra conductive solder from flowing within the package so as to cause a trouble such as short-circuiting. In addition, and more importantly, since the extent of the solder spreading can be accurately determined, it is also possible to precisely determine the necessary and sufficient amount of solder. Accordingly, if the necessary and sufficient amount of solder are given, the solder can be sufficiently supplied and spread over the confined area. It is a matter of course that any one of the above mentioned various arrangements can be used alone, but also, two or more of the above mentioned various arrangements can be used in combination.

The above mentioned packaged semiconductor device can be very easily assembled into an assemble circuit board 100 of the microstrip line structure having a plurality of signal conductors or circuit pattern conductors 100A formed on an upper surface thereof and a ground plane 100B formed on an under surface thereof, as shown in Figure 6.

Namely, an opening 100C sufficient to receive the cap portion of the packaged semiconductor device is formed through the assemble circuit board 100, and the cap portion of the packaged semiconductor device is inserted into the opening 100C in such a manner that the lead pins 7 are located at the side of the circuit pattern conductors 100A. In this condition, each of the lead pins 7 can be connected to a corresponding one of the plurality of circuit pattern conductors 100A through a solder 200A located on the circuit pattern conductors 100A, and the cap portion formed of the side wall 3 and the lid structure 40 can be connected to the ground plane 100B by a solder 200B which is filled into a gap formed between the cap of the package and an inner surface of the opening 100C and which extends over the ground plane 100B. With this assembling, since the back electrode 1C of the IC chip 1 is electrically connected to the cap portion formed of the side wall 3 and the lid structure 40, the lead pins 7 can be connected to the circuit pattern conductors 100A with a minimum distance, and the back electrode 1C of the IC chip 1 is connected to the ground plane 100B with a minimum distance.

Referring to Figure 7, there is shown a diagram-

matic sectional view of a modification of the packaged semiconductor device shown in Figure 2. In Figure 7, elements similar to those shown in Figure 2 are given the same Reference Numerals, and explanation thereof will be omitted for simplification of description.

As will be seen from comparison between Figures 2 and 7, the shown modification is characterized in that the lid structure 40 is formed of a first lid member 41B having a concave upper surface formed of a partial spherical surface and a second lid member 42B having a convex lower surface formed of a partial spherical surface, which is substantially complementary to the concave upper surface of the first lid member 41B.

In the case that the first and second lid members 41 and 42 are formed of a simple planar plate as shown in Figure 2, when it is attempted to uniformly spread the solders 50 for the purpose of fixing the lid members, it is necessary to press the lid members while accurately maintaining the lid members in a horizontal condition. However, this is actually difficult. This operation can be made simple and easy, by cooperation of the smooth curved upper surface of the first lid member 41B and the smooth curved under surface of the first lid member 42B, since it no longer necessary to accurately maintain the lid members in a horizontal condition. In addition, if the radius of curvature in the smooth curved upper surface of the first lid member 41B is made smaller than that in the smooth curved under surface of the first lid member 42B, when the pressure is applied to the lid members, the solder 50 can be effectively collected to a center region of the concave upper surface of the lid member 41B so that the solder can be pushed out through the via holes 44 by the convex lower surface of the lid member 42B. Accordingly, this arrangement makes it possible to manufacture the packaged semiconductor device on the basis of a mass production.

Referring to Figure 8A, there is shown a diagrammatic sectional view of a second embodiment of the packaged semiconductor device in accordance with the present invention. In Figure 8A, elements similar or corresponding to those shown in Figure 2 are given the same Reference Numerals, and explanation thereof will be omitted.

As will be apparent from comparison between Figures 2 and 8A, the structure of a portion "A" under a level somewhat lower than the level of the upper end of the side wall in the second embodiment is substantially similar to a corresponding portion of the first embodiment shown in Figure 2, but the second embodiment is similar to the conventional example shown in Figure 1 in that the side wall is covered with the rid of a single plate.

However, as shown in an exploded sectional view of Figure 8C, a step 30 is formed on an upper end of a side wall 3A so that the upper end 30A of an inside portion of the side wall 3A is lower than the upper end 30D of an outside portion of the side wall 3A. In addition, a step 40 is correspondingly formed at a lower side of a periphery of a lid plate 4A so that the lid plate 4A can be fitted onto the stepped upper end of a side wall 3A. Furthermore, a contact plate 10 in the form of a lead frame is located on and contacted to the faced-up back surface of the IC chip 1 with a periphery of the contact plate 10 being sandwiched and fixed between the lower surface of the lid plate 4A and the upper end 30A of the inside portion of the side wall 3A.

As shown in Figure 8B, this contact plate 10 has a central region 10A having a size substantially corresponding to the back surface of the IC chip 1, and a plurality of legs 10B radially outwardly extending from the central region 10A, like lead pins of a lead frame. The overall size of the contact plate 10 is slightly smaller than the size determined by the contour of the step 30, in order to ensure that the plurality of legs 10B can be smoothly put on the upper end 30A of the inside portion of the side wall 3A.

As shown in Figures 8A and 8C, the central region 10A of the contact plate 10 is bent downward from the plurality of legs 10B. In other words, the plurality of legs 10B of the contact plate 10 is bent slightly upward from the central region 10A of the contact plate 10.

In addition, if the plurality of legs 10B of the contact plate 10 is previously bent to a suitable degree as shown in Figure 8C, when the lid plate 4A is fitted and fixed to the side wall 3A, the plurality of legs 10B of the contact plate 10 are caused to be resiliently deformed between the faced-up back surface of the IC chip 1 and the cap formed of the side wall 3A and the lid plate 4A, so as to ensure a mechanical contact and an electrical connection between the contact plate 10 and the faced-up back surface of the IC chip 1 in the case that the back surface of the IC chip 1 is not previously bonded to the central region 10A of the contact plate 10.

Now, a process for manufacturing the packaged semiconductor device shown in Figure 8A will be explained with reference to Figure 8C.

For example, firstly, the back surface of the IC chip 1 is bonded to the central region 10A of the contact plate 10, and then, solder bumps 9 are located on contact pads formed on the upper surface of the IC chip 1. The IC chip thus prepared is bonded facedown on the substrate 2 which has been assembled with the side wall 3A and the lead pins 7, so that the bumps 9 are directly above corresponding connection pads 6 formed on the substrate 1 and the plurality of legs 10B are put on the upper end 30A of the inside portion of the side wall 3A.

Thereafter, pre-formed solder bumps 5 are put on the upper end surface of the outside portion of the side wall 3A, and then, the lid plate 4A is fitted onto

the upper end of the side wall 3A so that the step 40 of the lid plate 4A is fitted with the step 30 of the side wall 3A. Suitable heat and pressure are applied onto the lid plate 4A so as to force the lid plate 4A to the side wall 3A, so that the lid plate 4A is bonded to the upper end of the side wall 4A by the solder 5, and simultaneously, with the legs 10B of the contact plate 10 are sandwiched and fixed between the lower surface of the lid plate 4A and the upper end 30A of the inside portion of the side wall 3A. Thus, the air-tight package is completed, and at the same time, the faced-up back surface of the IC chip 1 is electrically connected through the contact plate 10 to the cap formed of the side wall 3A and the lid plate 4A, and the contact plate 10 is sandwiched and fixed between the side wall 3A and the lid plate 4A.

As will be apparent from the above, the packaged semiconductor device in accordance with the present invention is characterized in that the IC chip is packaged in the flip-chip bonding with using no bonding wire, and also, the back electrode of the IC chip is electrically connected to the metallic cap of the package. Accordingly, the back electrode of the IC chip can be electrically connected to a ground plane of a microstrip line structure through the metallic cap of the package, and since no bonding wire is used, it is possible to prevent deterioration of the IC chip which would otherwise be caused by the bonding wires.

In other words, the packaged semiconductor device suitable to microstrip line structure can be realized with using no bonding wire, and in accordance with the flip-chip bonding.

Therefore, the packaged semiconductor device in accordance with the present invention can be used in a microstrip line structure indispensable to a low noise amplifier. Accordingly, a high performance semiconductor device which can be used in a microwave band, can manufactured inexpensively and at a high productivity.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

Claims

1. A packaged semiconductor device comprising:

an insulating substrate (2) having a first surface formed with a plurality of connection pads (6) and a second surface formed with a plurality of external connection members (7) each of which is electrically connected to a corresponding one of said connection pads (6) through a via hole (2A) formed through said insulating substrate (2);

an integrated circuit chip (1) bonded face-down on said first surface of said insulating substrate (2) so that said integrated circuit chip (1) is electrically connected to said connection pads (6) through solder bumps (9), said integrated circuit chip (1) having a back electrode (1C) formed on a back surface (1B) thereof; and

an electrically conductive cap (3, 41, 42; 3, 41B, 42B; 3A, 4A) covered on said first surface of said insulating substrate (2) so that said integrated circuit chip (1) is encapsulated in a space defined by said insulating substrate and said conductive cap,

said back electrode (1C) of said integrated circuit chip (1) being electrically connected to said conductive cap.

2. A packaged semiconductor device claimed in Claim 1 wherein said back electrode (1C) of said integrated circuit chip (1) is electrically connected through an electrically conducting element (50A; 10) to said conductive cap.

3. A packaged semiconductor device claimed in Claim 2 wherein said conductive cap is composed of a side wall (3A) bonded at its lower end to said insulating substrate (2) so as to surround said integrated circuit chip and a lid plate (4A) bonded to an upper end of said side wall, and wherein said electrically conducting element is formed of a contact plate (10) having a central region (10A) mechanically and electrically connected to said back electrode (1C) of said integrated circuit chip (1), said contact plate (10) also including a peripheral portion sandwiched and electrically connected between said lid plate (4A) and said upper end of said side wall (3A).

4. A packaged semiconductor device claimed in Claim 3 wherein said contact plate (10) is in the form of a lead frame having a plurality of legs (10B) radially outwardly extending from said central region (10A), a tip end of each of said plurality of legs (10B) being sandwiched and electrically connected between said lid plate (4A) and said upper end of said side wall (3A).

5. A packaged semiconductor device claimed in Claim 2 wherein said conductive cap is composed of a side wall (3) bonded at its lower end to said insulating substrate (2) so as to surround said integrated circuit chip and a lid structure (40) bonded to an upper end of said side wall, said lid structure (40) being bonded and electrically connected to said back electrode (1C) of said integrated circuit chip (1) through a solder (50A).

6. A packaged semiconductor device claimed in

Claim 5 wherein said lid structure (40) includes a first lid member (41) bonded to said upper end of said side wall, said first lid member (41) having a plurality of via holes (44) formed through said first lid member (41), and a second lid member (42) bonded to said first lid member (41) through a solder (50), said solder (50) filling said via holes (44) and extending to a lower surface of said first lid member (41) so as to mutually bond said said first lid member (41) and said back electrode (1C) of said integrated circuit chip (1).

FIGURE 1 PRIOR ART

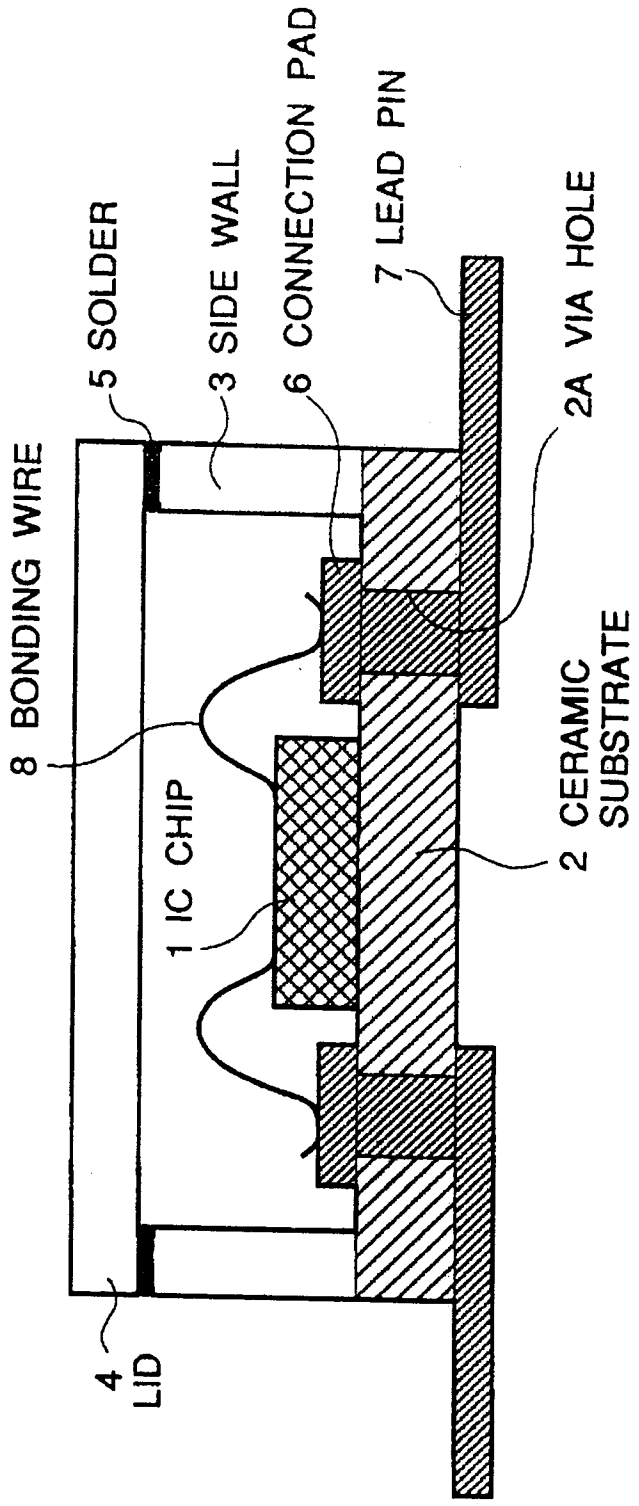


FIGURE 2

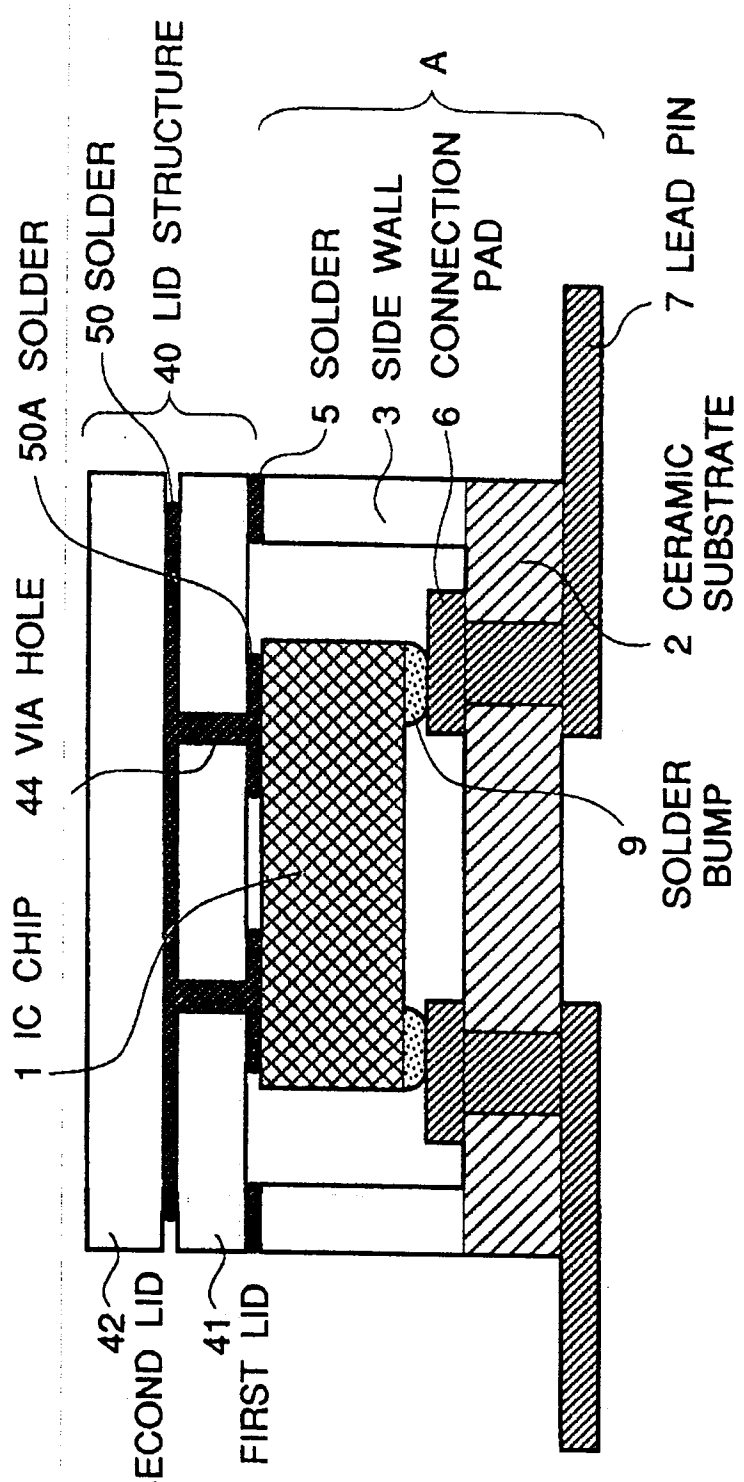

1 IC CHIP
44 VIA HOLE
50A SOLDER
50 SOLDER
40 LID STRUCTURE
5 SOLDER
3 SIDE WALL
6 CONNECTION PAD
A
7 LEAD PIN
2 CERAMIC SUBSTRATE
9 SOLDER BUMP
42 SECOND LID
41 FIRST LID

FIGURE 3A

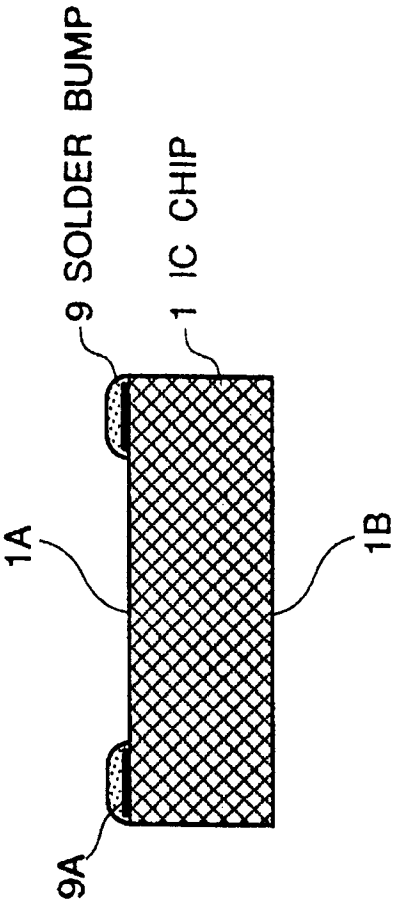


FIGURE 3B

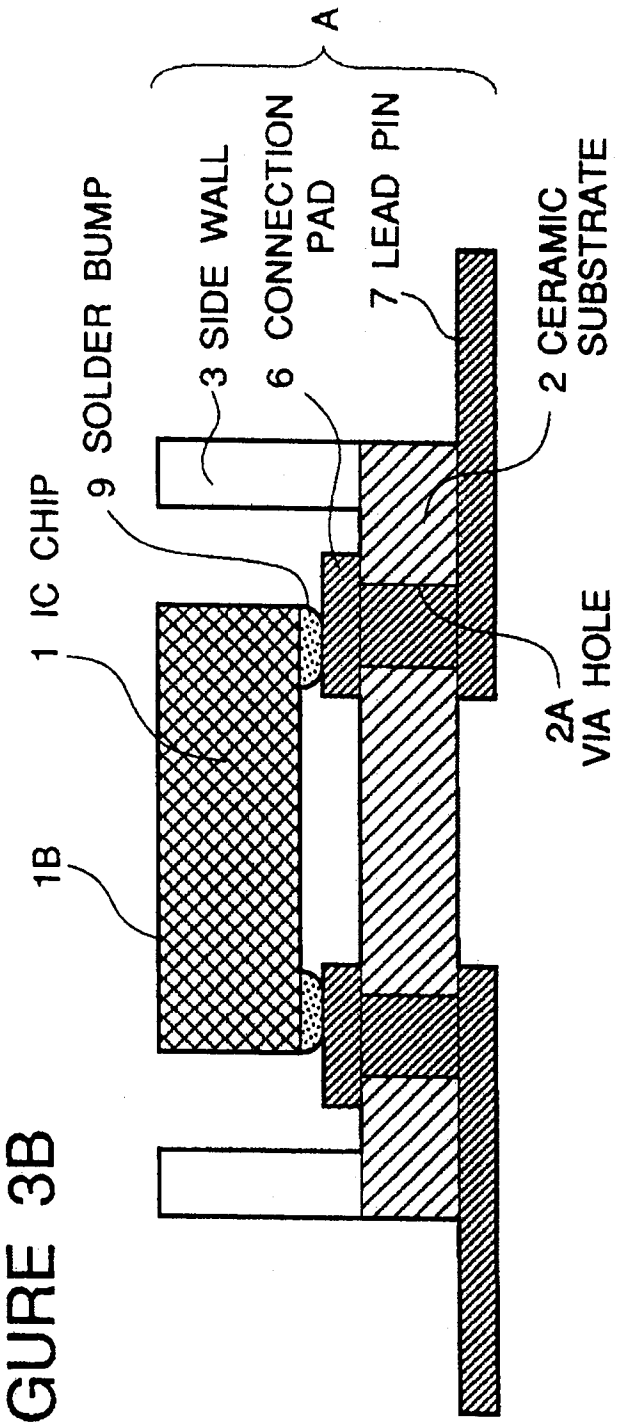


FIGURE 3C

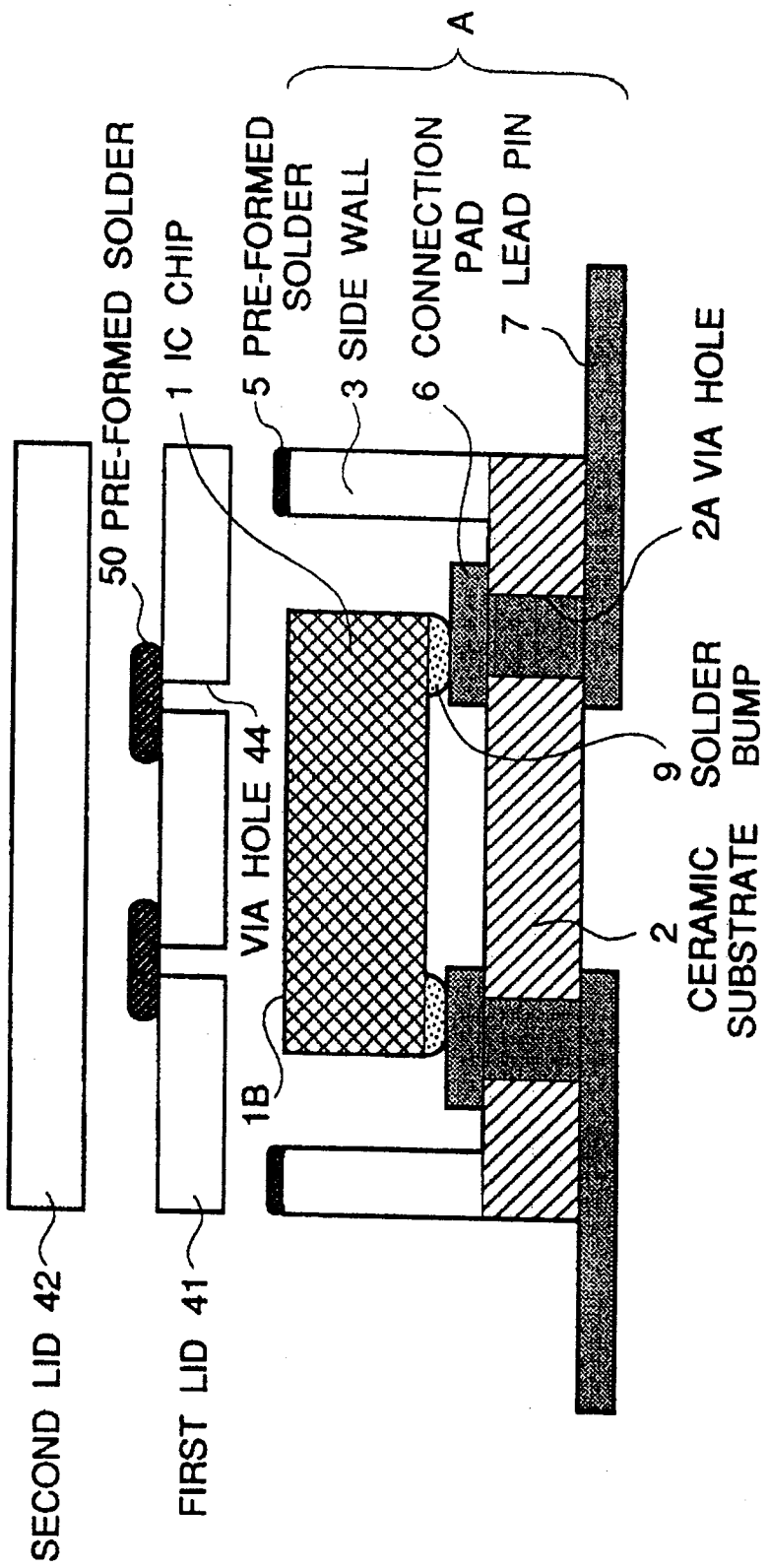

SECOND LID 42
FIRST LID 41
50 PRE-FORMED SOLDER
1 IC CHIP
1B
VIA HOLE 44
5 PRE-FORMED SOLDER
3 SIDE WALL
6 CONNECTION PAD
7 LEAD PIN
A
2A VIA HOLE
9 SOLDER BUMP
2 CERAMIC SUBSTRATE

FIGURE 4A

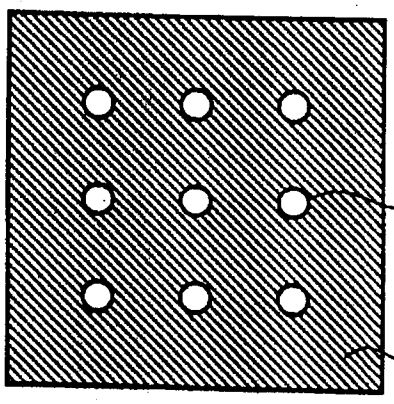


FIGURE 4B

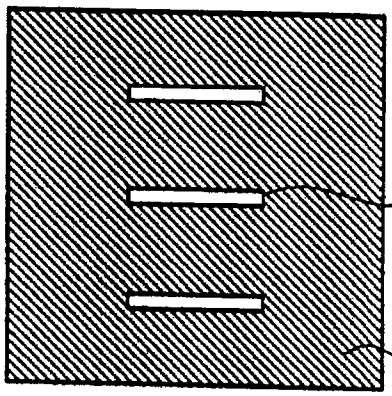


FIGURE 4C

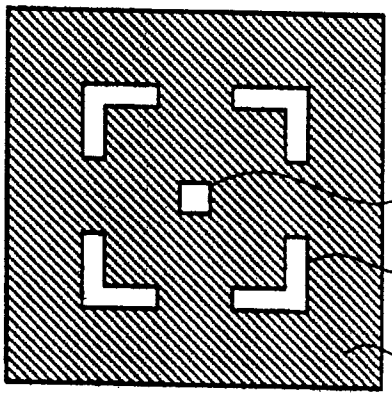


FIGURE 4D

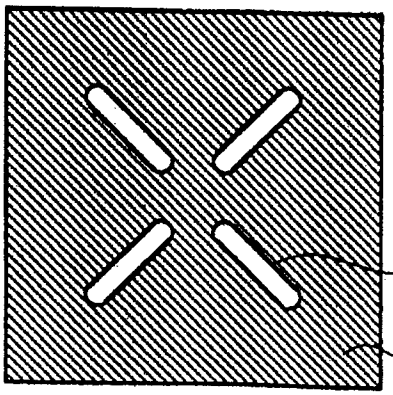


FIGURE 5A

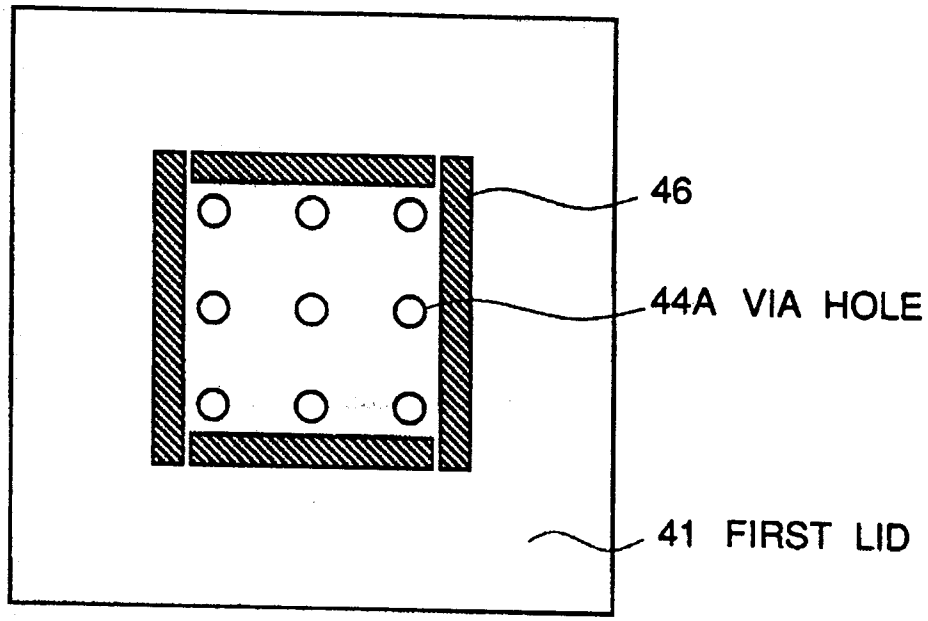


FIGURE 5B

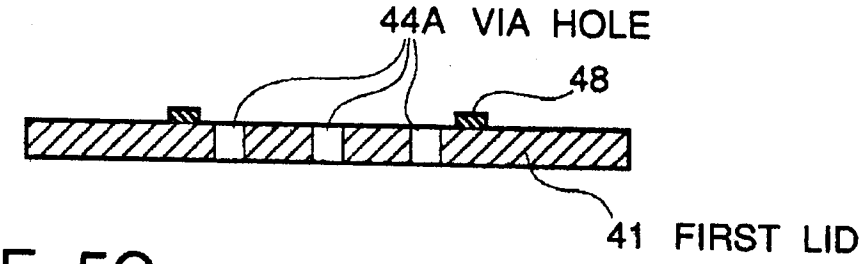


FIGURE 5C

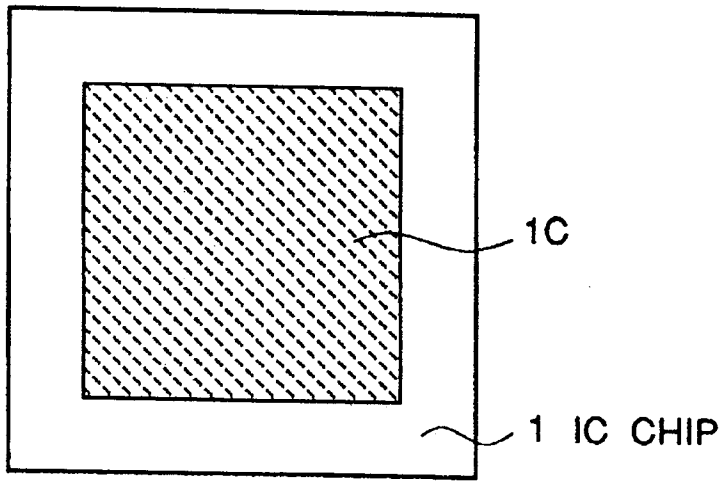


FIGURE 6

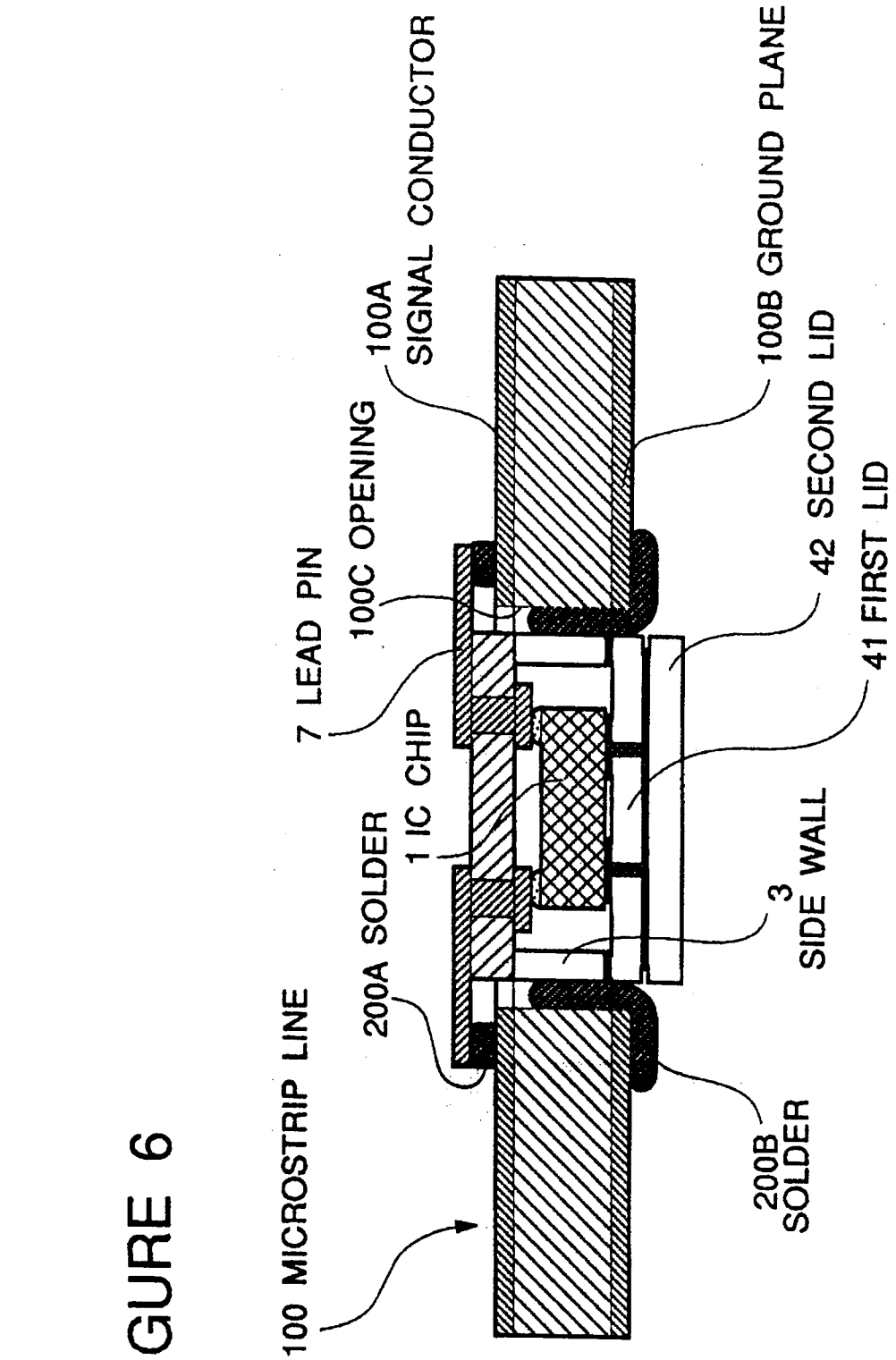
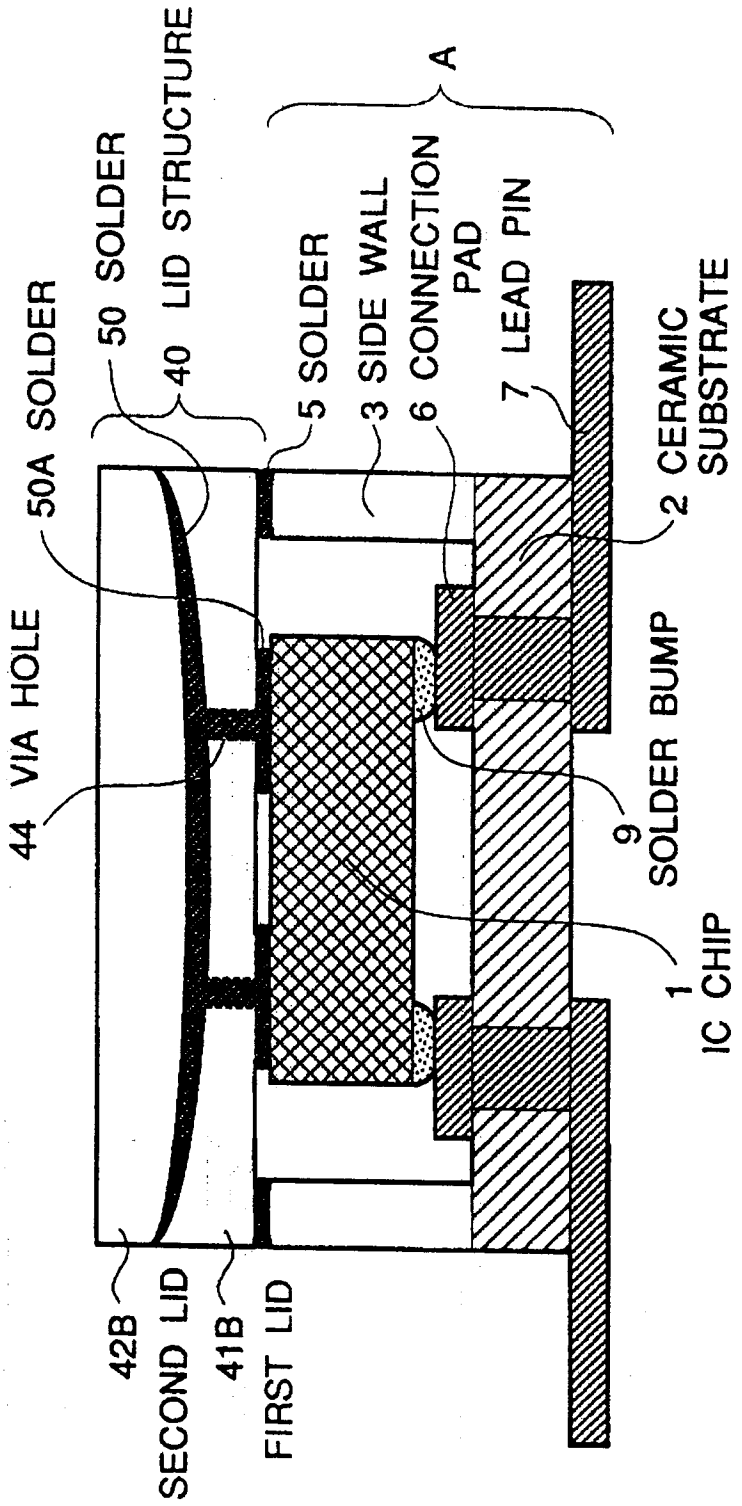

100 MICROSTRIP LINE
200A SOLDER
1 IC CHIP
7 LEAD PIN
100C OPENING
100A SIGNAL CONDUCTOR
100B GROUND PLANE
42 SECOND LID
41 FIRST LID
3 SIDE WALL
200B SOLDER

FIGURE 7


44 VIA HOLE
50A SOLDER
50 SOLDER
40 LID STRUCTURE
5 SOLDER
3 SIDE WALL
6 CONNECTION PAD
7 LEAD PIN
A
2 CERAMIC SUBSTRATE
9 SOLDER BUMP
1 IC CHIP
42B SECOND LID
41B FIRST LID

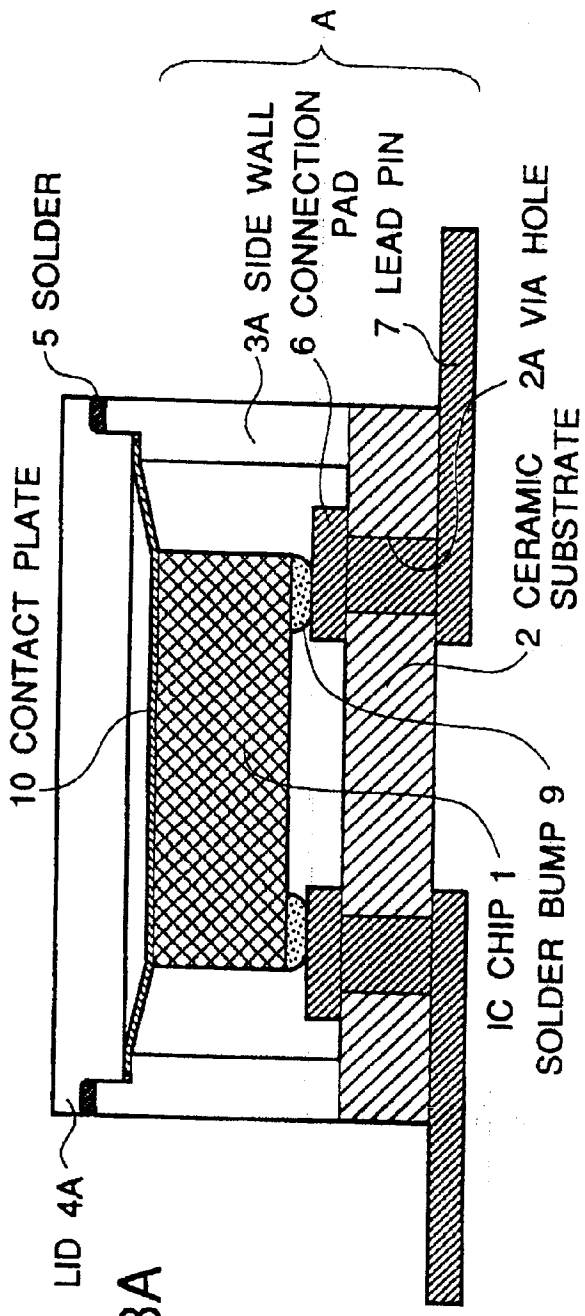


FIGURE 8A

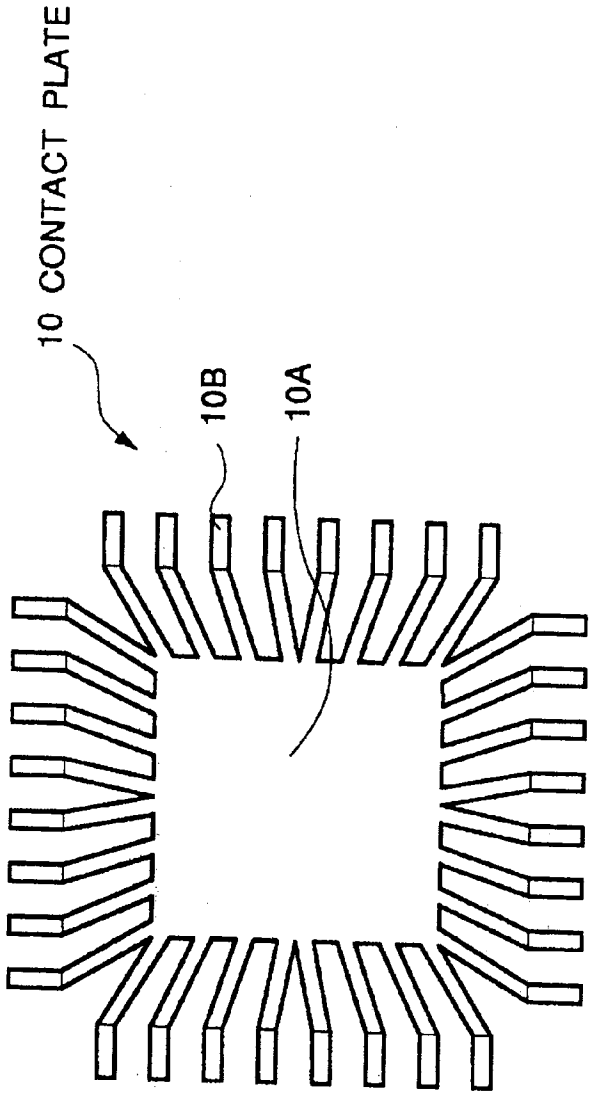
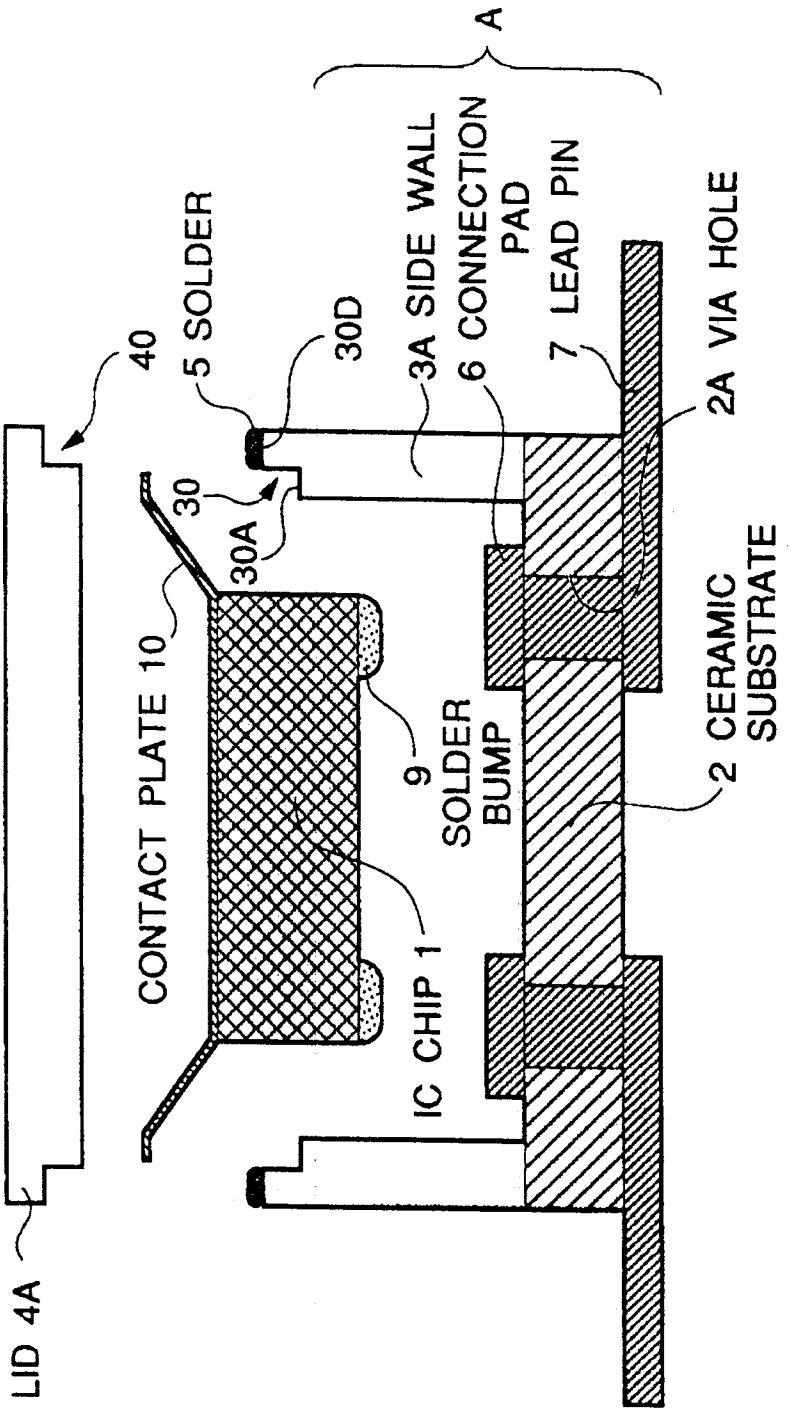


FIGURE 8B

FIGURE 8C


A
40
5 SOLDER
30D
3A SIDE WALL
6 CONNECTION PAD
7 LEAD PIN
2A VIA HOLE
30
30A
CONTACT PLATE 10
9 SOLDER BUMP
2 CERAMIC SUBSTRATE
IC CHIP 1
LID 4A

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(54) Packaged semiconductor device suitable to be mounted and connected to microstrip line structure board.

(57) A packaged semiconductor device comprises an insulating substrate (2) having an upper surface formed with a plurality of connection pads (6) and an under surface formed with a plurality of external connection members (7) each of which is electrically connected to a corresponding one of the connection pads (4) through a via hole (2A) formed through the insulating substrate (2). An integrated circuit chip (1) is bonded facedown on the upper surface of the insulating substrate (2) so that the integrated circuit chip (1) is electrically connected to the connection pads (6) through solder bumps (9). An electrically conductive cap (3, 41, 42) is covered on the first surface of the insulating substrate (2) so that the integrated circuit chip (1) is encapsulated in a space defined by the insulating substrate and the conductive cap. A back electrode of the integrated circuit chip (1) is electrically connected to the conductive cap.through an electrically conducting element (50A).

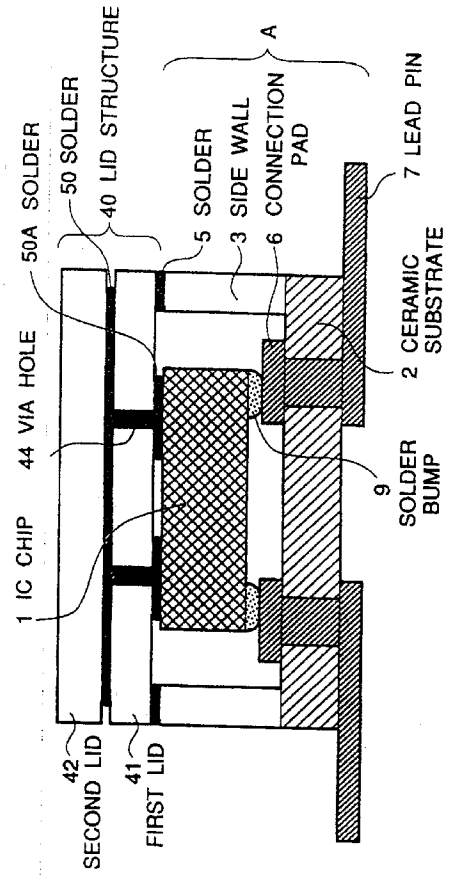

FIGURE 2

EP 0 615 289 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 40 0530

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	US-A-5 166 773 (GENERAL ELECTRIC) * column 8, line 10 - line 22; claim 1; figure 14 *	1,2	H01L23/055 H01L23/04 H01L23/498
A		3,5	

A	IBM TECHNICAL DISCLOSURE BULLETIN, vol.31, no.4, September 1988, NEW YORK pages 37372 - 373 'thermal enhancement of thermal cap'		

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 February 1995	De Raeve, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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